Earth Science Technology Office (ESTO) Conference 2004

An architecture for a space-based reconfigurable protocol chip

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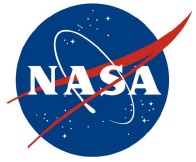
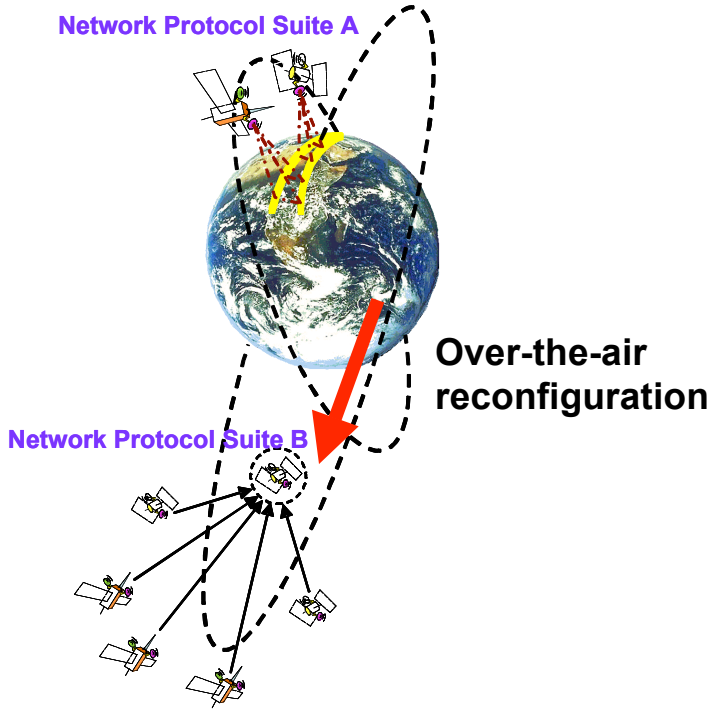
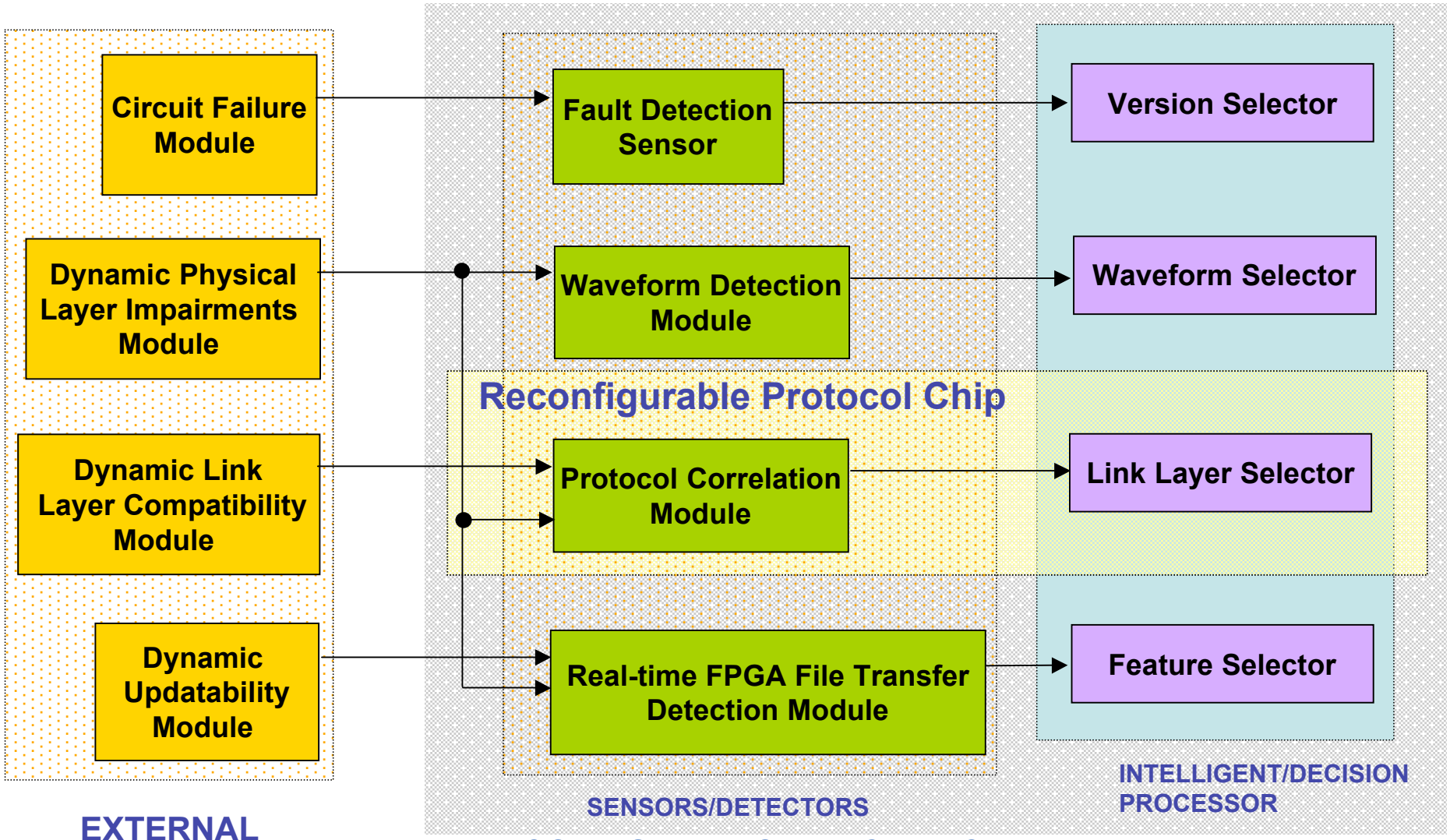


- **Technical Objectives**
  - The reconfigurable protocol chip concept
    - Autonomous reconfiguration for heterogeneous network operation
    - Over-the air reconfiguration for long-life infrastructure



Stimulus & Space-based Reconfiguration Architecture

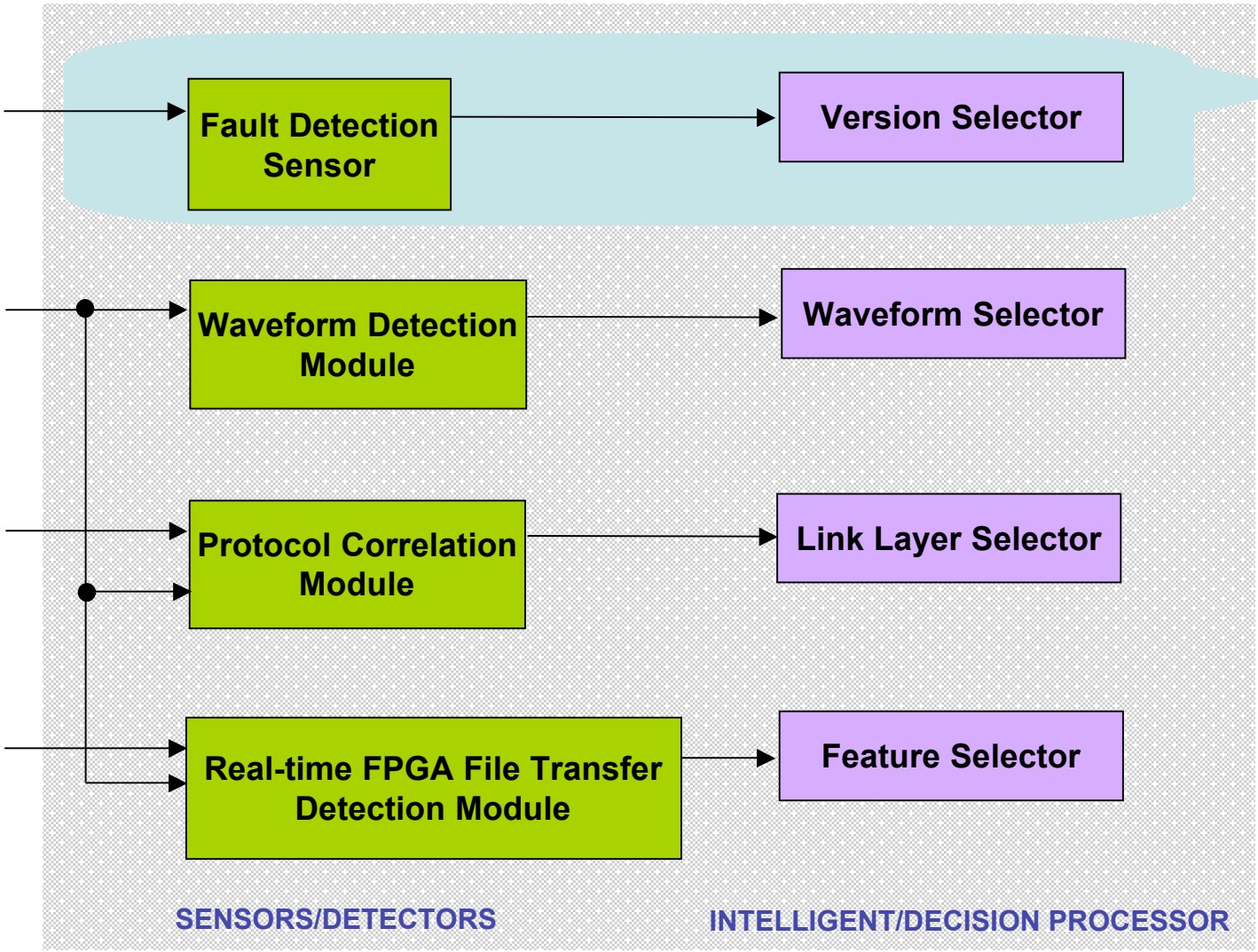


RECONFIGURATION ARCHITECTURE
(4 Parts – Fault, Waveform, Protocol, Feature)

External Stimulus

- Space-based Reconfiguration Model Circuit Failure Module
  - Radiation is key source of system fault in space environment (from presentation by Raphael Some, JPL): Galactic Cosmic Rays (GSM), Solar Radiation (e.g. Solar Wind/Protons, Coronal Mass Ejections), Planetary Magnetic Fields (e.g. Van Allen Belts, Jovian belts)
  - Key types of radiation effects
    - Total Ionization Dose (TID): cumulative ionization causing increase in leakage current and threshold shifts
    - Single Event Effects (SEE): single particles, Linear Energy Transfer, Single Event Latch up (SEL), Single Event Upset (SEU), Single Event Multiple Upset (SEMU), Single Event Gate Rupture, Single Event Micro-dose
- Characterize the key impairment in space (and the effect it has on performance at the physical layer, assume RF links)
  - Ideally map to EIRP (perform link budget, map to potential set of waveforms or allowable waveforms, then perform appropriate detection in Waveform Detection Module). Out of scope on current effort, recommend future studies be performed to scope this work (i.e. what is the expected set of waveforms in space?)
  - Our approach: Assume BPSK waveform.
- Characterize the key attributes that distinguish a link layer protocol
  - Use the Goddard Space Flight Center (GSFC) Parallel Integrated Frame Synchronizer (PIFS) Chip as a baseline capability. The PIFS Chip has the capability to synchronize to HDLC (RFC 1662), 802.3, and GFP link layer framing.
- Version upgrades, added features, reliability of valid transfer is captured.
  - Out of scope. However, work in this area being performed in parallel at JPL by Savio Chao and under an IND Adaptive Rate Protocol task. We leverage some aspects for us in our architecture. This task will monitor the work to maintain relevance between tasks.

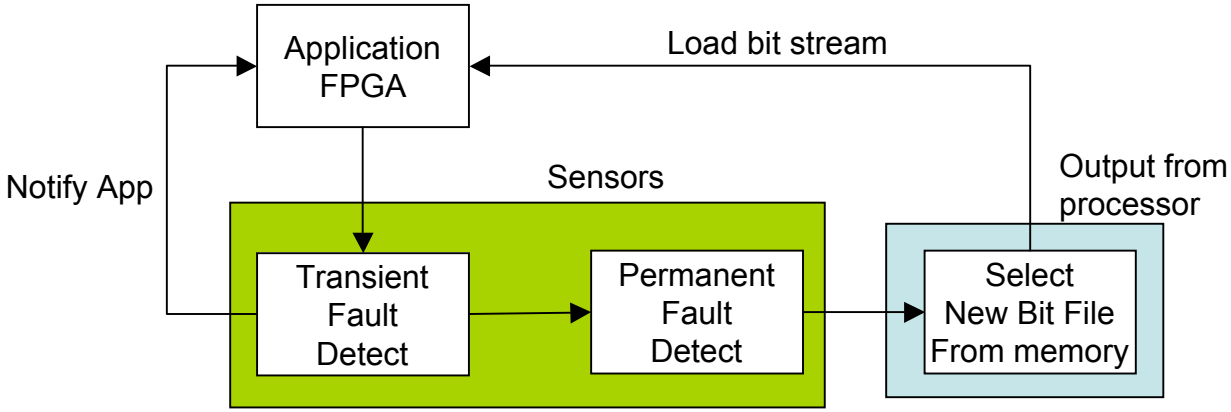
Space-based Reconfiguration Architecture



Part 1: FAULT DETECTION ARCHITECTURE (Sensor + Selector)

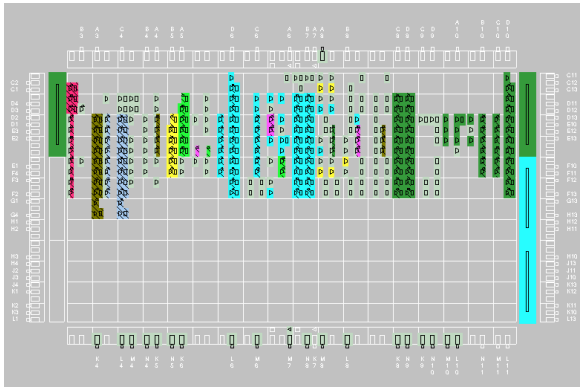
- **Focus is on permanent failures within FPGA**
- **Utilize spatial variation of FPGA mapping**

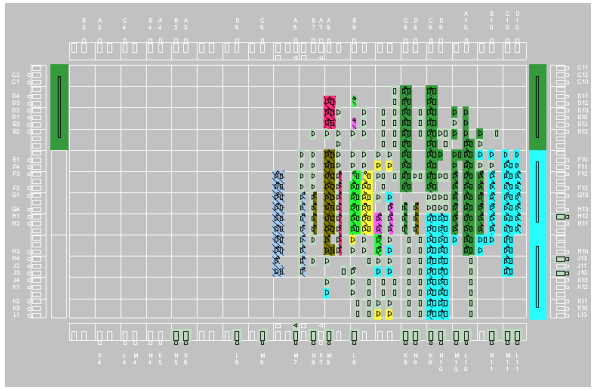
- **Fault Tolerance Mapping**
  - Two tiered fault diagnosis and recovery steps

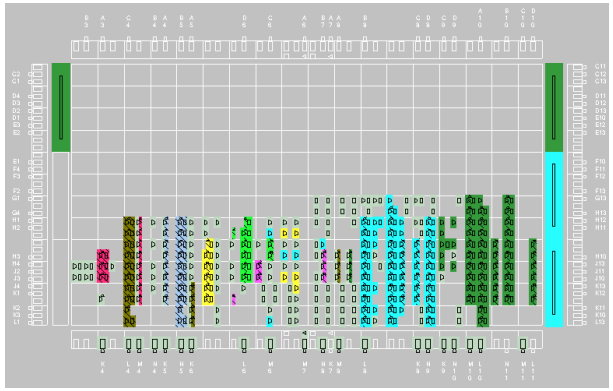


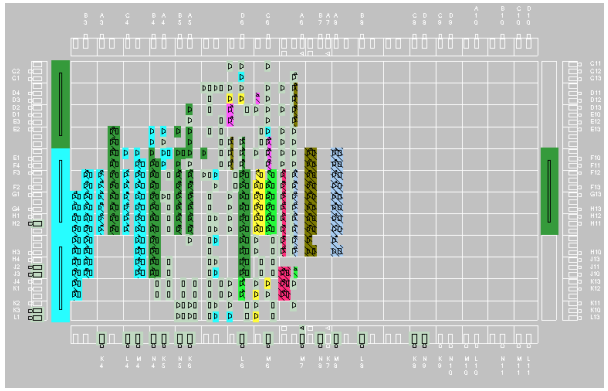
- Transient Detect: Cyclic Redundancy Check (CRC) failure
- Permanent Detect: Multiple consecutive CRC failures
- Triple Modular Redundancy (TMR) may require too much resources. Will rely on higher layers to deal with transient error effects.

- Fault Tolerance Mapping (continued)
  - Sample protocol processing design with 50% utilization, using spatial variation of FPGA

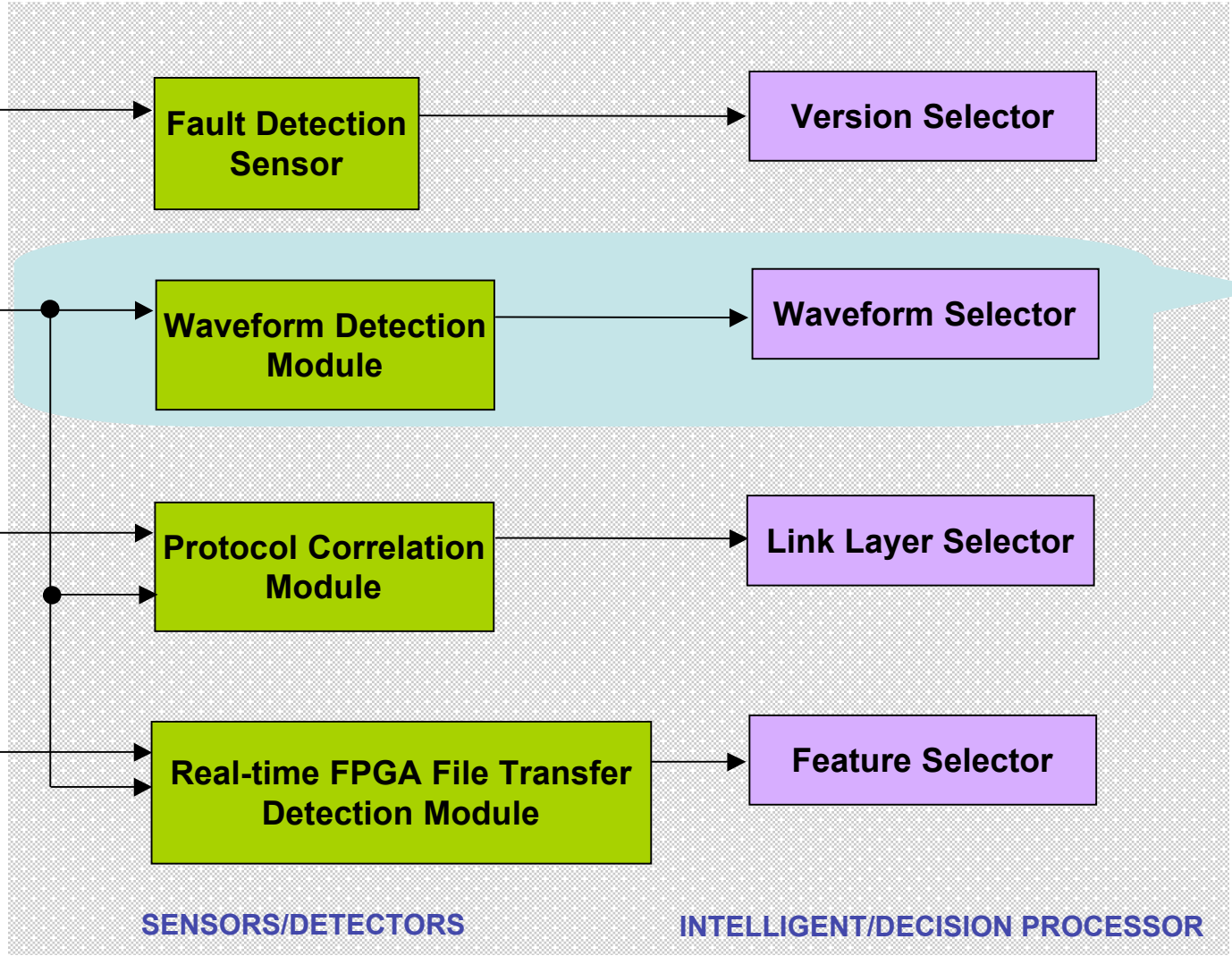








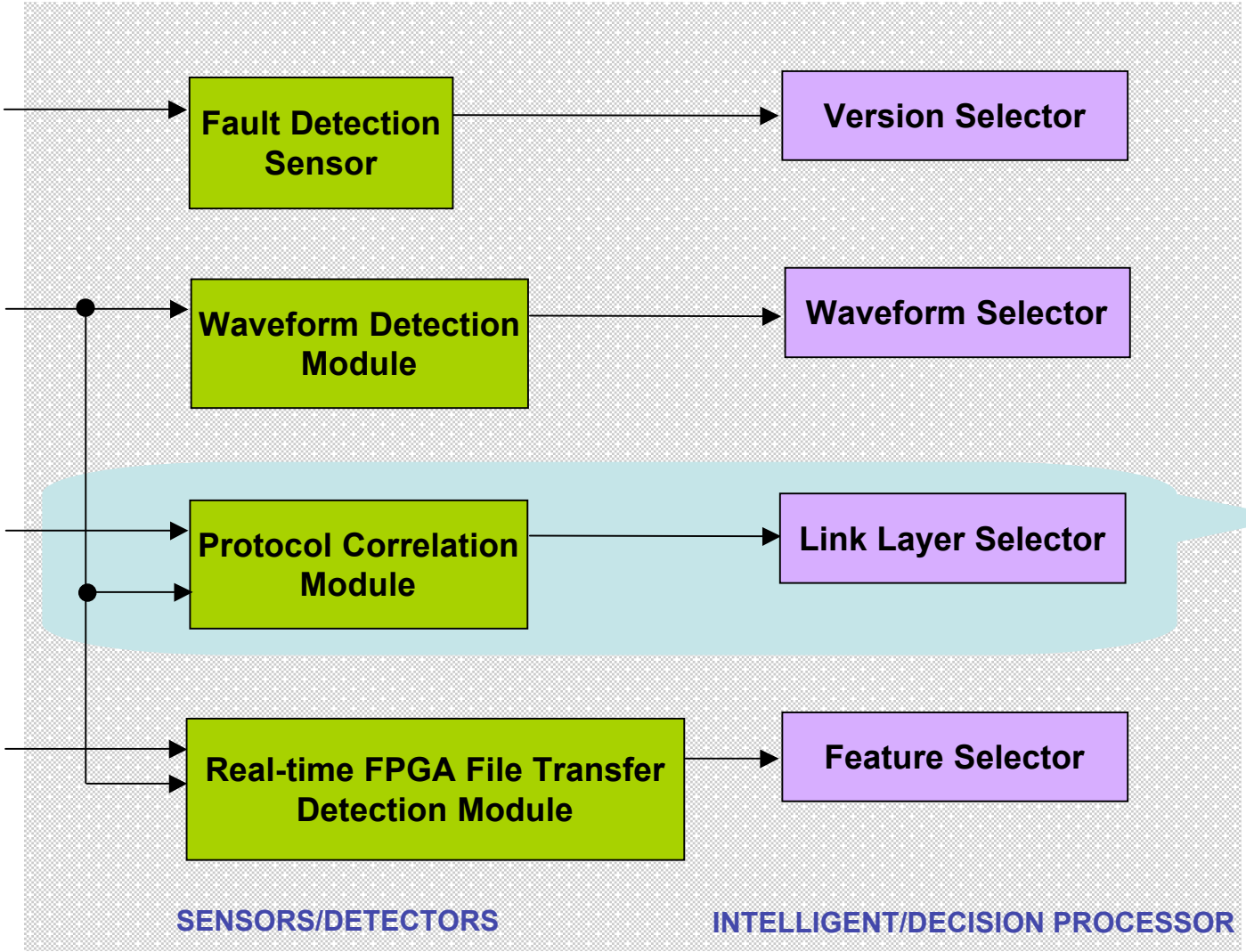
Space-based Reconfiguration Architecture



Part 2: WAVEFORM ARCHITECTURE (Sensor + Selector)

- Assume **BPSK** (future work might involve examining a set of waveforms and selecting optimal waveform for link closure similar to a dial-up modem)
- e.g. Monitor work under the Software Defined Radio (SDR) Forum and the Software Communications Architecture (SCA)

Space-based Reconfiguration Architecture



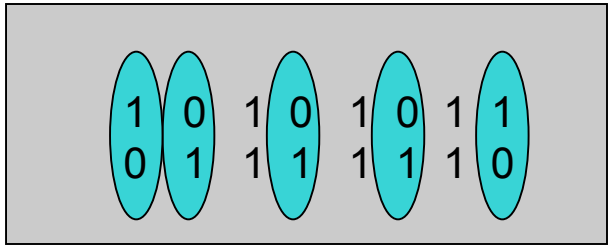
Part 3: PROTOCOL ARCHITECTURE (Sensor + Selector)

- Detect and Select between
  - **RFC 1662 (HDLC)**
  - **802.3**
  - **Generalized Framing Procedure (GFP)**

• Link Layer Recognition and Processing Schemes

– Consider standards: RFC1662 (HDLC), 802.3, and GFP

Use standard majority rule to decide between 802.3 header (AB hex) and HDLC header (7E).



Identify unique bits between two link layer formats

802.3

Preamble 56-bits	Start Frame 8–bits (AB)	Destination Address 48-bits	Source Address 48-bits	Length 16 -bits	LLC	Data 46 – 1500 bytes	Pad	FCS 32 bits

Opening Flag 8 –bits (7E)	Address Field 8 or 16-bits	Control 8 -bits	Data 8*N -bits	CRC 16 -bits	Stop Flag 8 –bits (7E)

RFC 1662 (HDLC)

- GFP is a common framing approach that is capable of carrying various traffic types across a SONET/SDH network or Optical Transport Network (OTN)
- Based on ITU-T Recommendation G.7041/Y.1303 where interfaces for G.709 is specified for OTN

GFP

	Core Header		Payload	Payload FCS
	PDU Length Indicator	Core Header Error Control (HEC) Field	4 to 65535 octets	Payload Frame Check Sequence
	2-octets	2-octets		4-octets

- GFP
  - cHEC is a CRC-16
  - Generator polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$

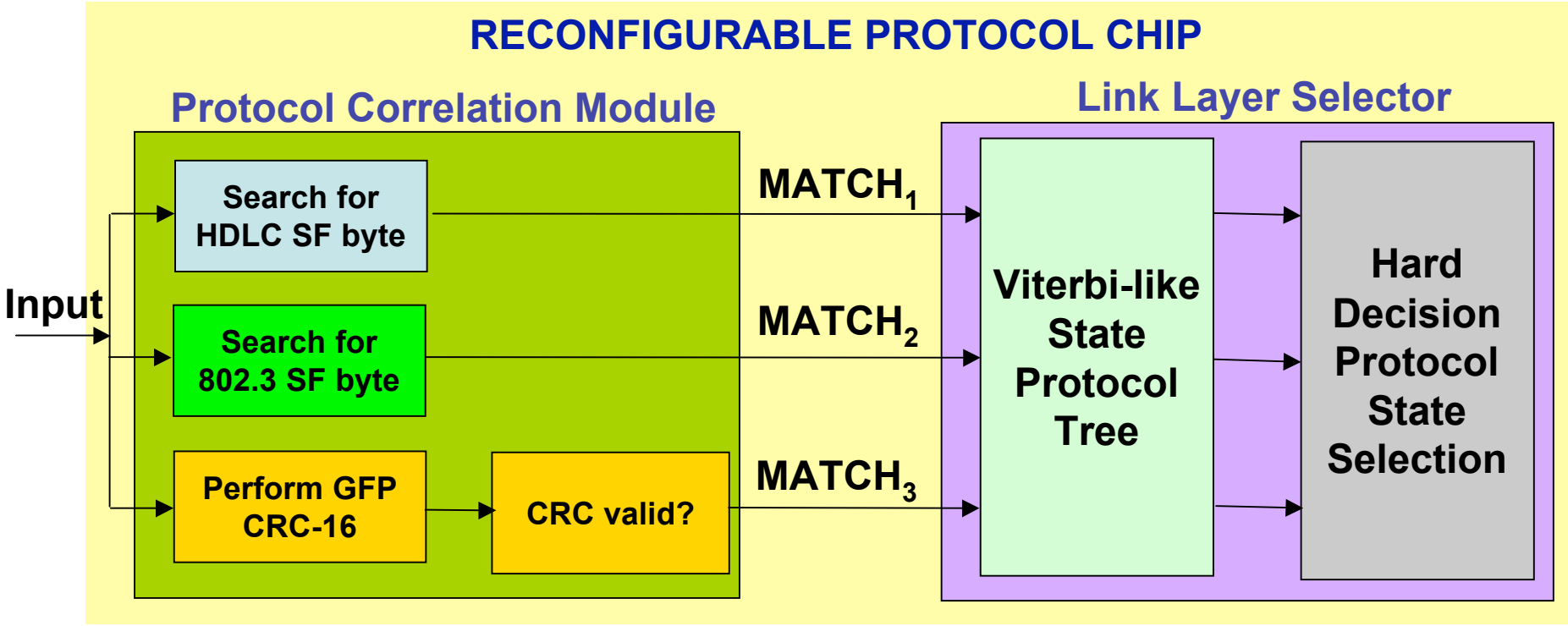
Combined Analysis: RFC 1662 (HDLC) and 802.3 versus GFP

• HDLC: Assuming equally likely frame sizes (16-bit patterns), then there are 256 (0x7E) patterns out of the 2^{16} -3 -1 = 65532 possible patterns for the length field that could result in a mistaken HDLC start -> 256/65532 = ~0.0039 likelihood (with no additional state knowledge, or use of CRC-16)
• 802.3: Similarly, there are 256 patterns out of the 65532 that can be incorrectly detected as mistaken 802.3 start
• However: utilizing the CRC-16, then this reduces the chance of detecting the GFP frame as either an HDLC or an 802.3 as1/65532 = 1.525e-5.
• Performing detection on multiple consecutive frames, the likelihood of false detection of n consecutive GFP frames as either an 802.3 or an HDLC is

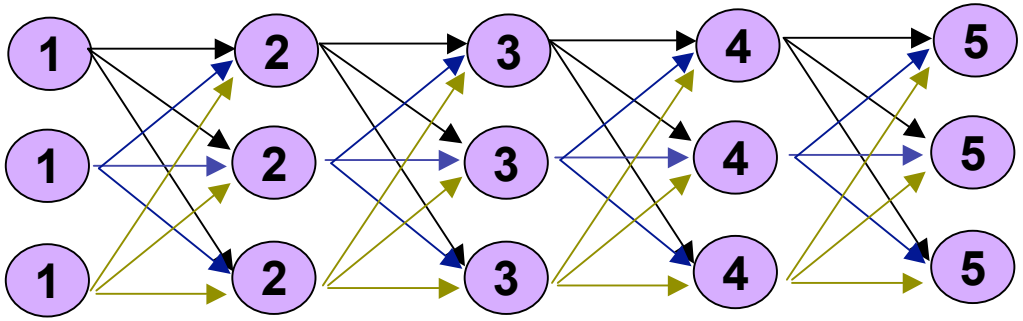
$$p = (1.525e-5)^n$$

• For n = 3, we have 3.55e-15

- SELECTED PROTOCOLS: ***RFC1662 (HDLC), 802.3, GFP***

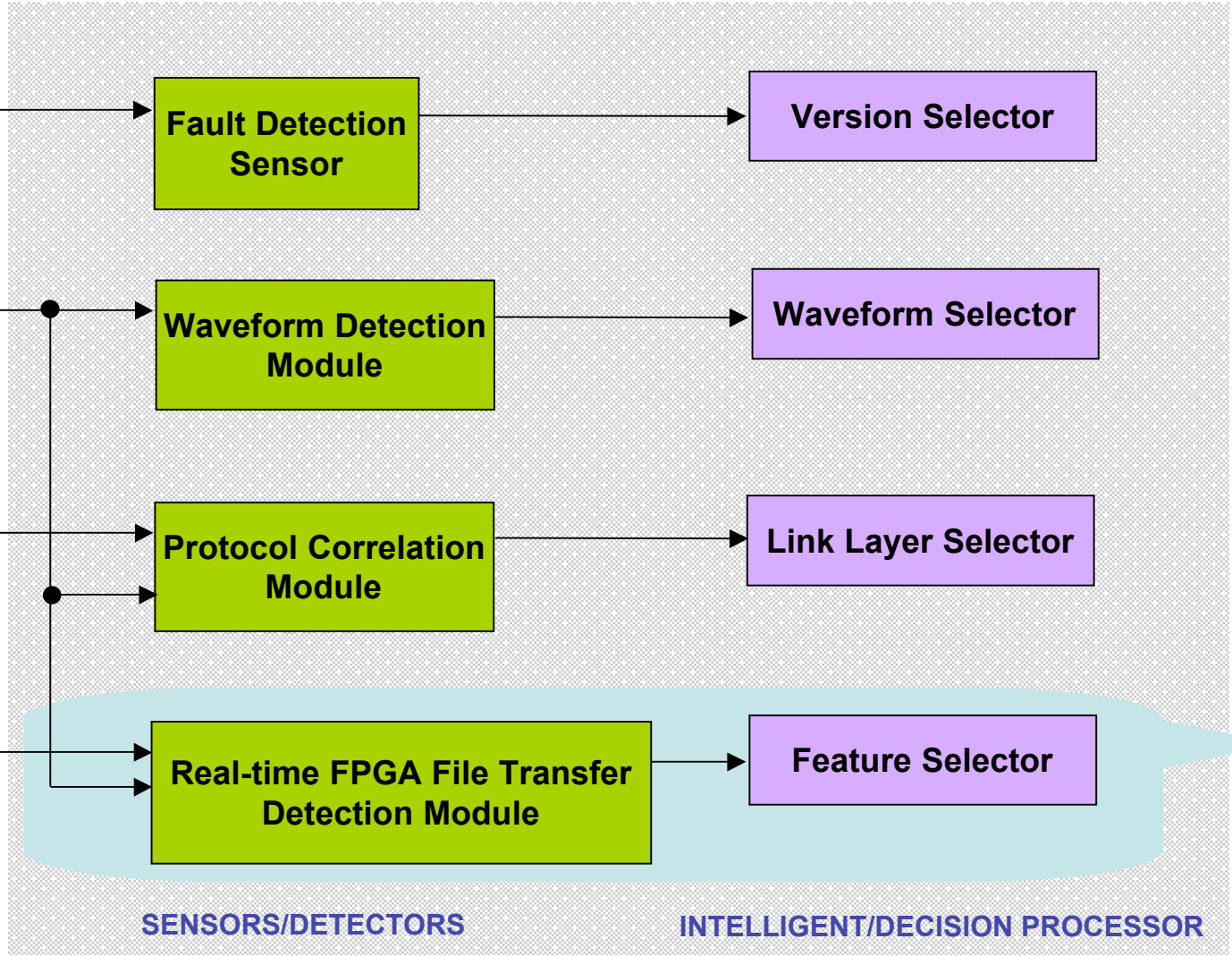


Viterbi Like State Protocol Tree (Selection performed after 5 state)



$$S_i(k) = S_i(k-1) + \sum_{j=1}^{3} w_{i,j} \times MATCH_j$$

Space-based Reconfiguration Architecture



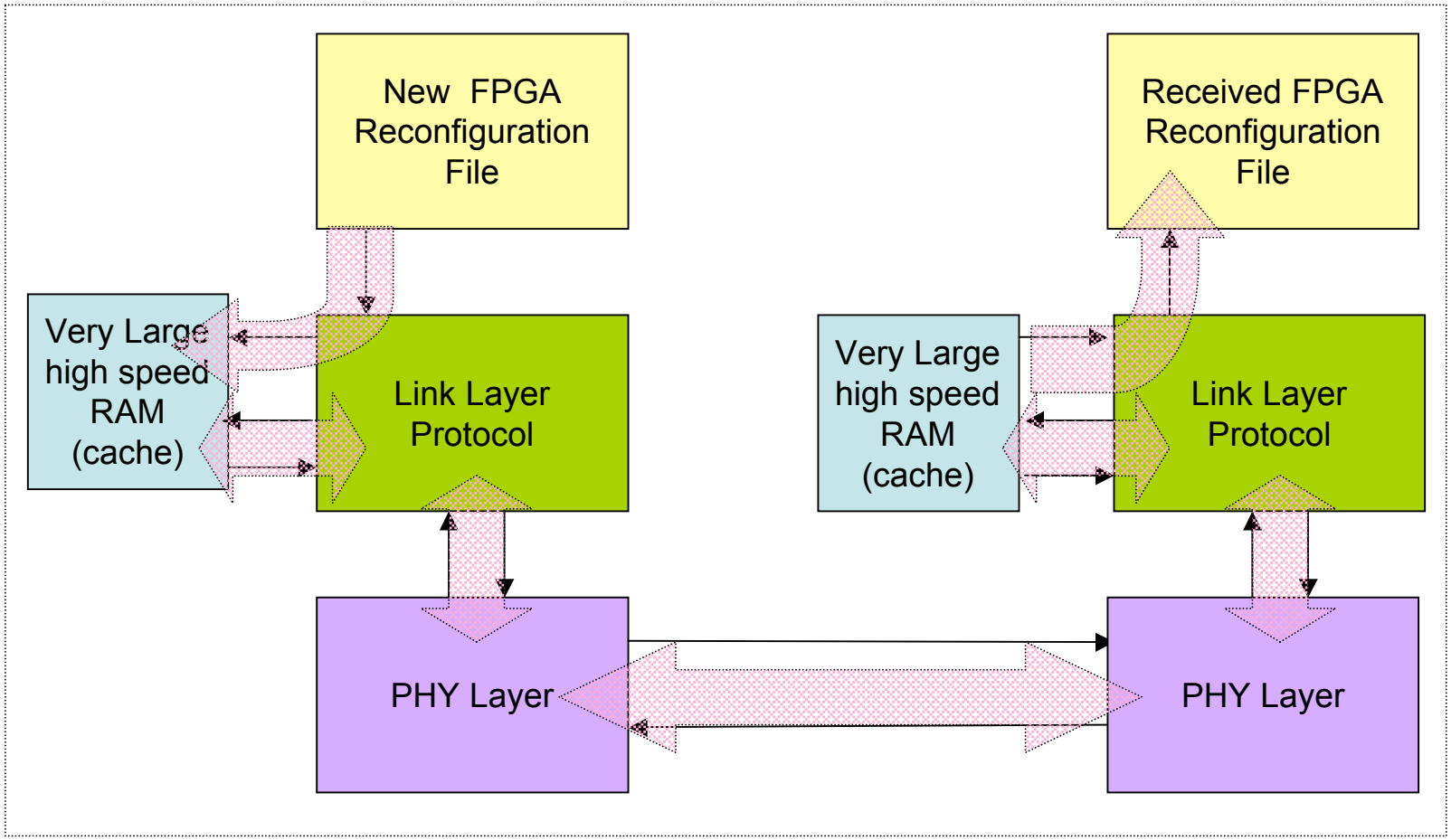
Part 4: FEATURE ARCHITECTURE (Sensor + Selector)

- Leverage IND Adaptive Rate Protocol research
- Leverage Savio Chau's application layer reconfiguration research

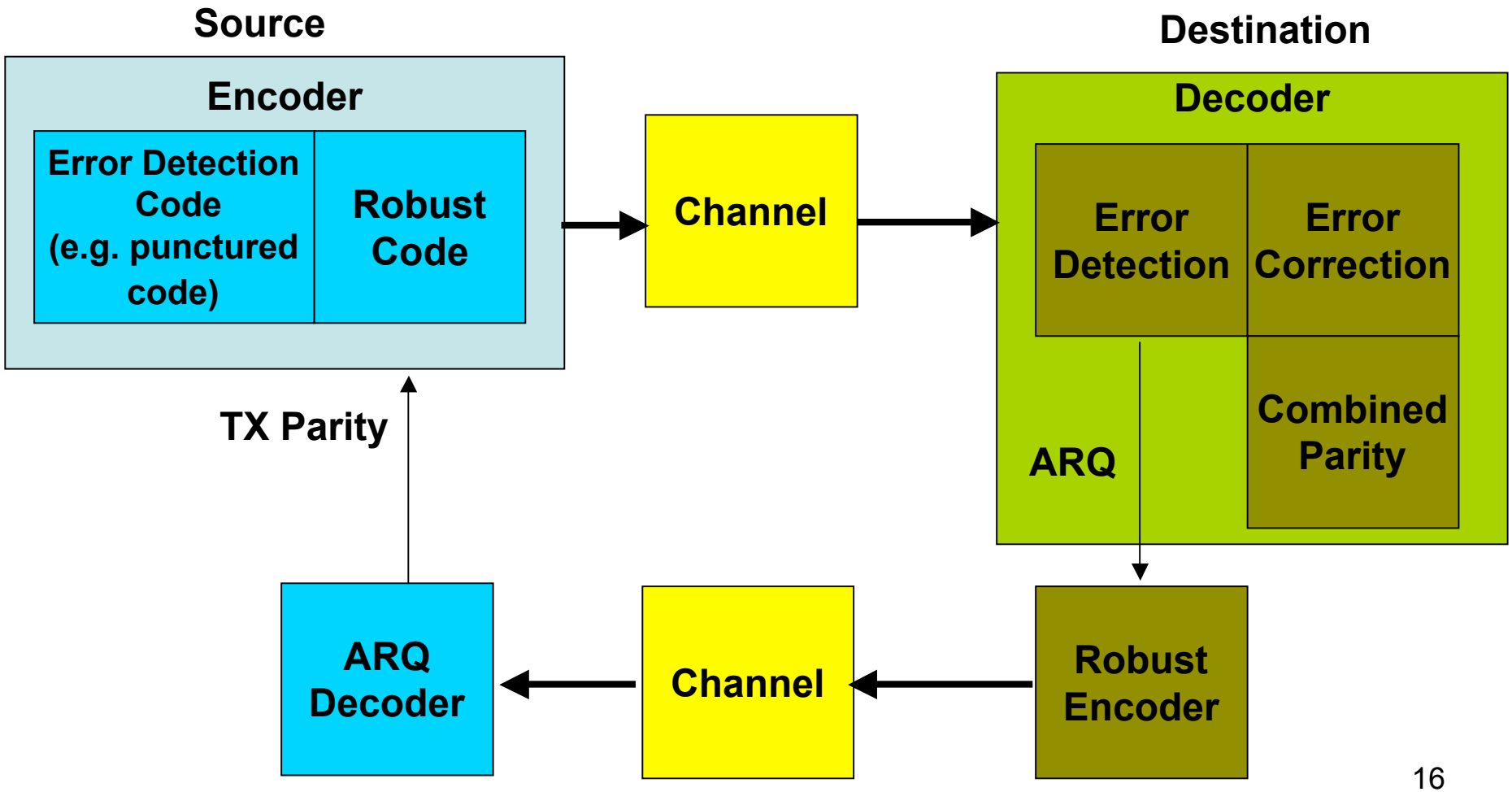
- Space-based Reconfiguration Architecture Model - Real-time FPGA File Transfer Module (FEATURE SELECTION)
  - Procedure for reliable FPGA File Transfer in Space (reliable link layer procedure developed)
    - Allows for ROBUST platform by enabling updates to current protocol core/procedures
    - Allows for UPGRADABILITY new protocols to be infused into the architecture
  - Leverage application layer reconfiguration command set described in [*] to allow for reliable in-situ wireless transfers.
  - **Joint work with New Jersey Institute of Technology**: Reliable Link Layer study performed in collaboration with Professor Roy You[#]

[*] Savio Chau, Adans Ko, Kar-Ming Cheung, “Mission Operation for Reconfigurable Spacecraft”, to be presented at SpaceOps 2004.
[#] Roy You, “Proximity Link with Hybrid ARQ”, June 2004, Technical Report.

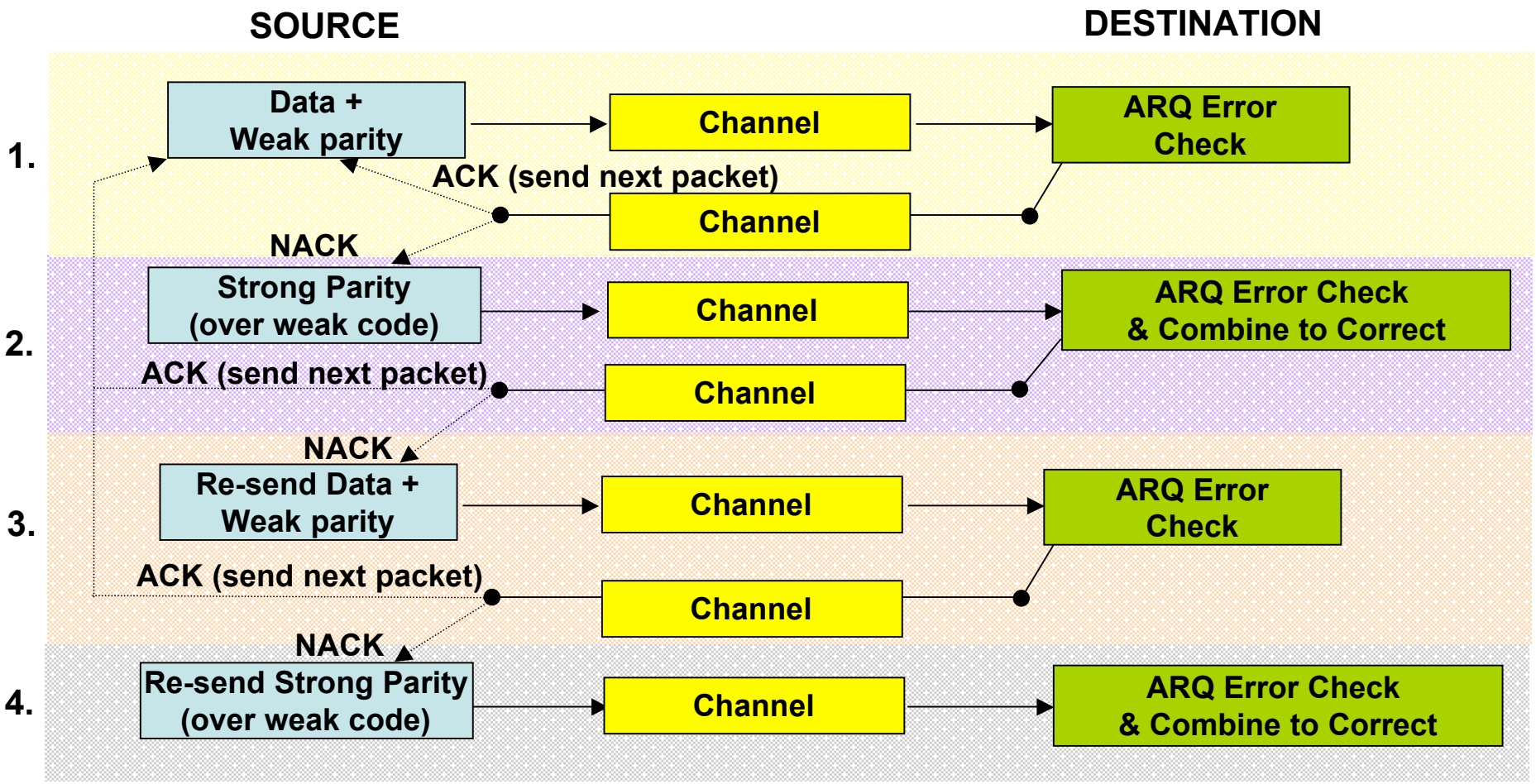
COTS Reconfigurable platforms ideal for prototyping
A reliable file transfer link layer protocol



Decompose the reliable link layer procedure into Source and Destination function block component



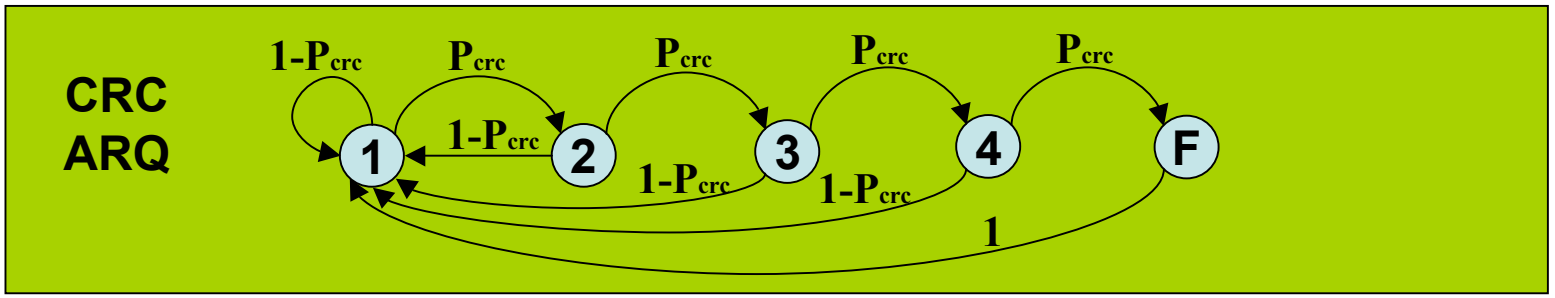
- **Develop a reliable link layer protocol utilizing Hybrid-ARQ methods**
  - **Numerous methods for implementing Hybrid ARQ – Selected method based on well-known Lin & Yu paper [%]**

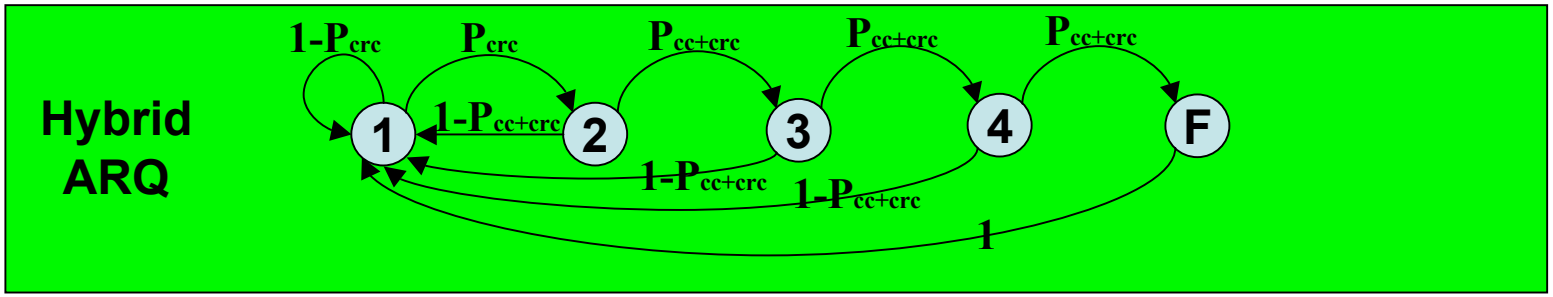


[%] S. Lin and P. Yu, "A hybrid ARQ scheme with parity retransmission for error control of satellite channels", IEEE Transactions on Communications, vol. 30, no. 7, July 1982.

Performance Analysis: Markov Chain

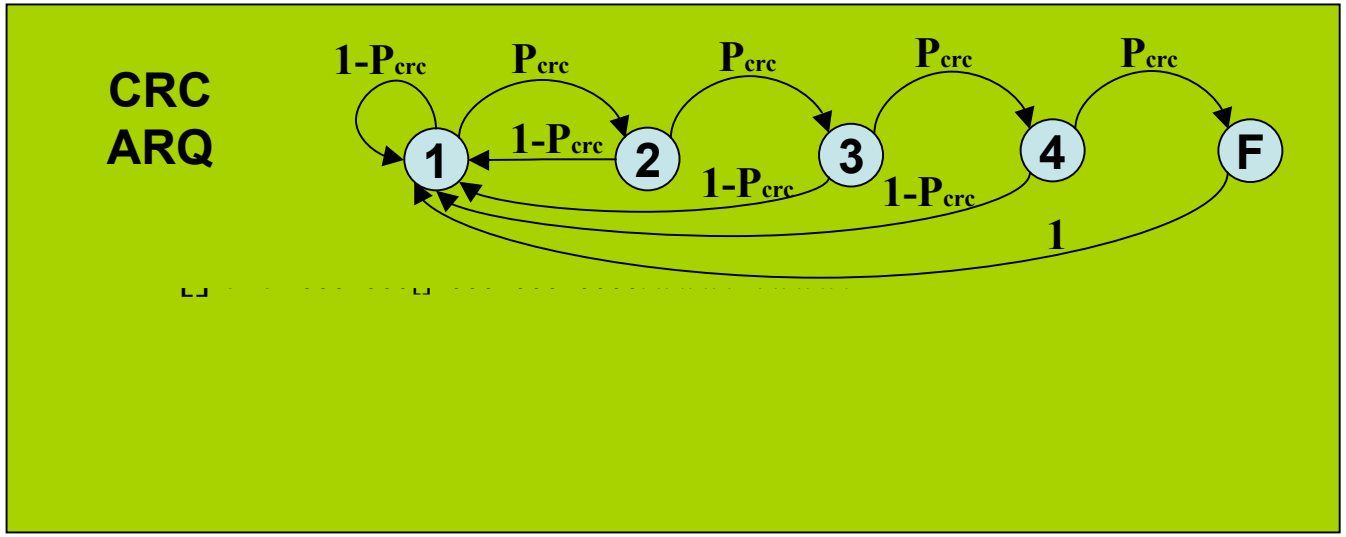
- The performance of CRC-ARQ and hybrid-ARQ can be compared using Markov Chain model.

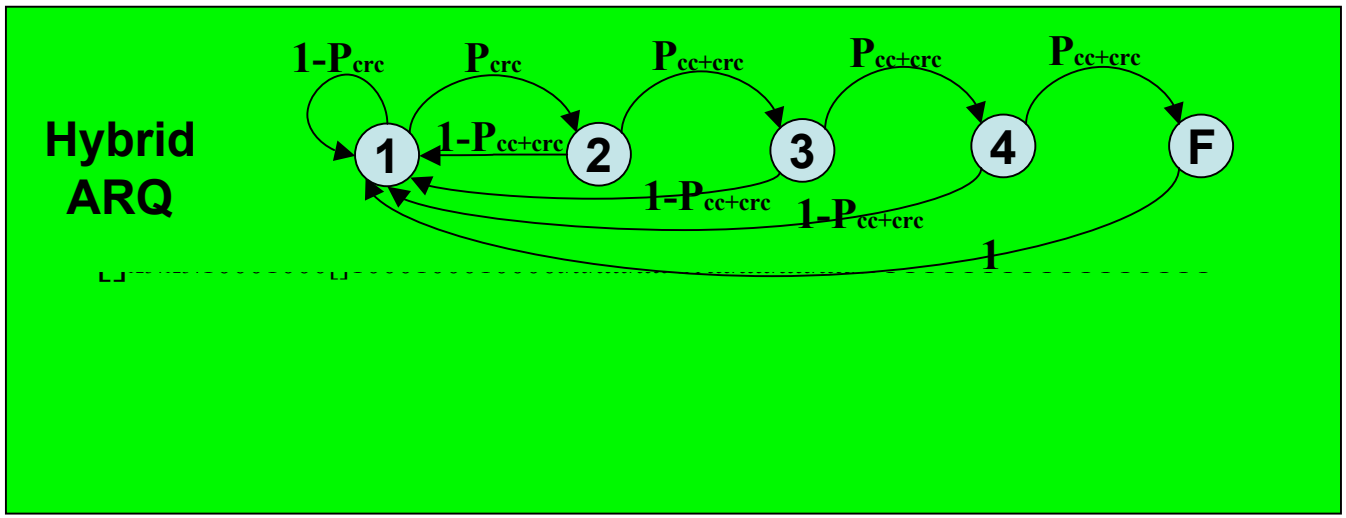




Performance Analysis: Steady State Equations

- The probability of each Markov state can be calculated

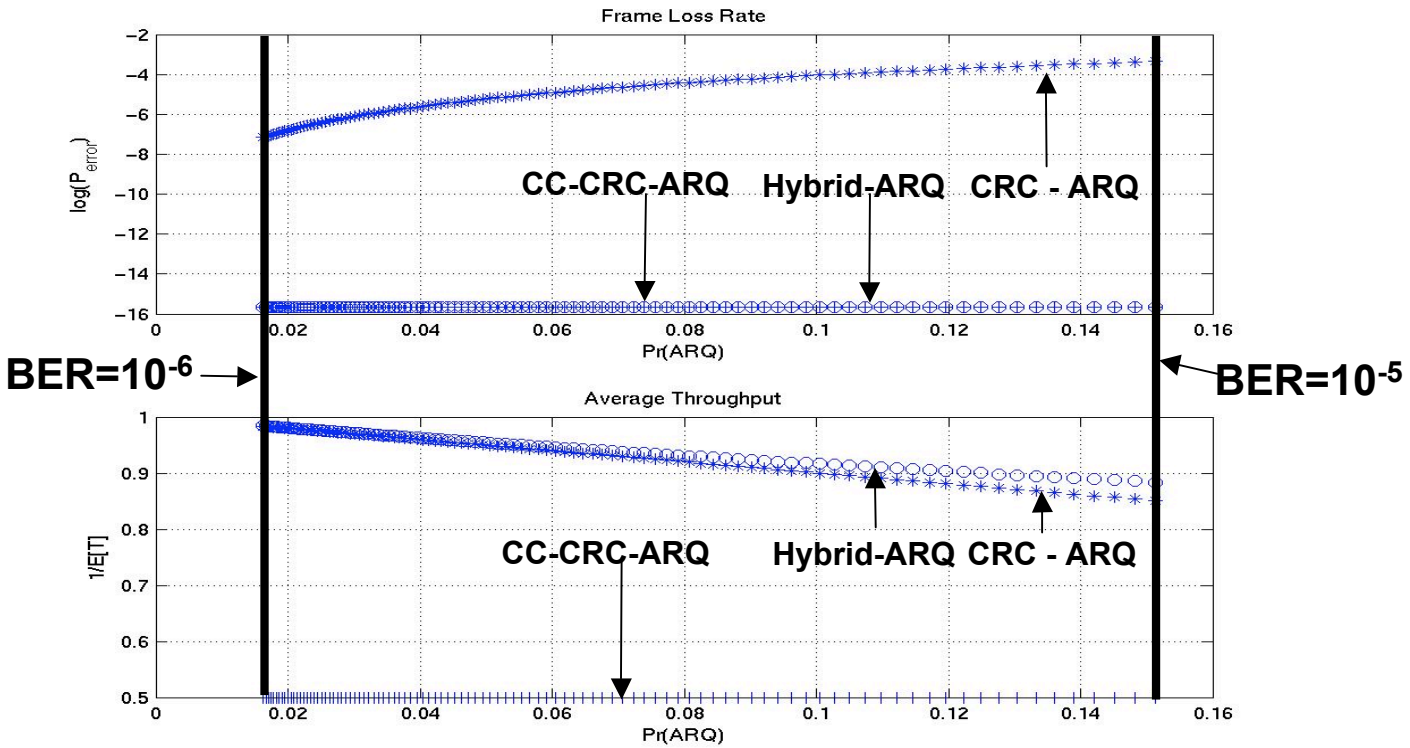




Average Transmission Time is

Average Frame Failure is

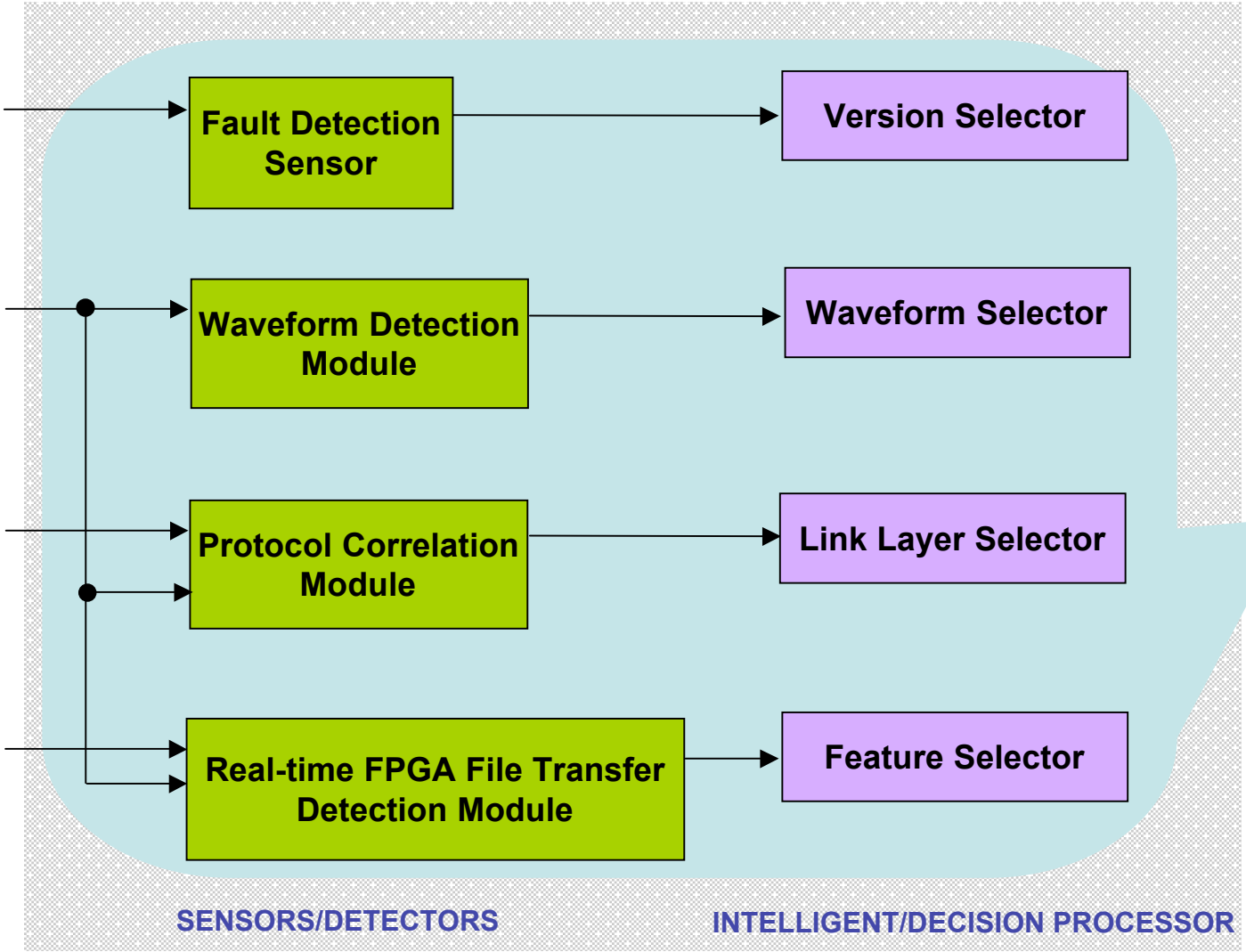
Part 4: Feature Architecture



	Error Performance	Throughput	Complexity
CRC - ARQ	10^{-5}	1	Low
Hybrid ARQ	10^{-15}	1	CC Code
CC-CRC	10^{-15}	1/2	CC Code

Provide better balance of throughput, and reliability

Space-based Reconfiguration Architecture



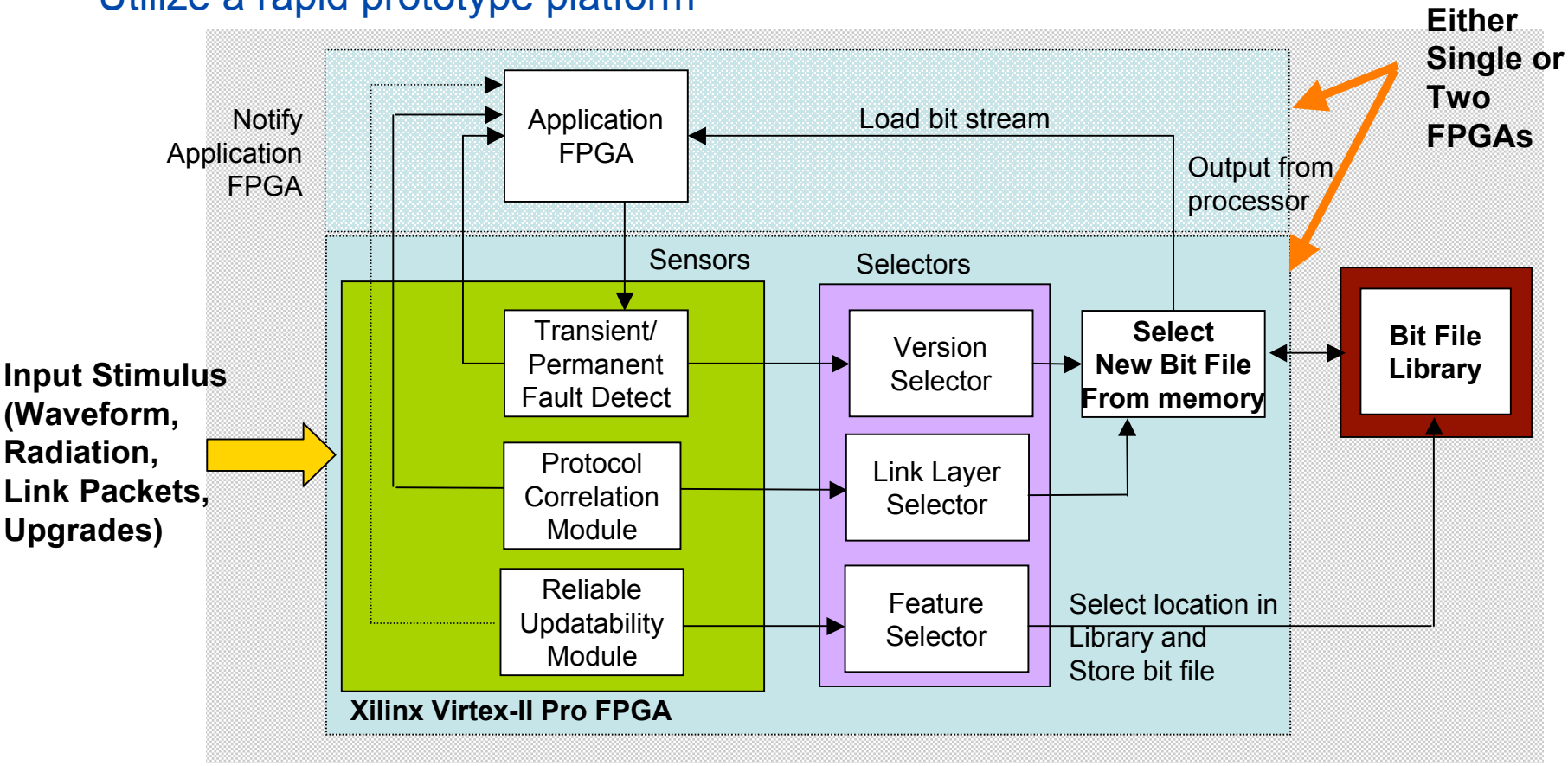
COMBINED ARCHITECTURE (Sensor + Selector)

- **HW description of combined 4 parts**

Overall HW Architecture

Reconfigurable Waveform/Link Protocol/Version/Updatability HW Platform

- Combined Sensing/Selection for Version (Fault), Waveform (BPSK default), Link Layer (RFC 1662, 802.3, GFP) and Feature (Reliable Updatability)
- Utilize a rapid prototype platform



Space-based Reconfiguration HW Architecture

- Refine our weighting calculations for our Protocol Sensor Detector
- Currently building the signal processing structure for the sensor for GFP, RFC1662, 802.3
- Provide partial reconfiguration capability

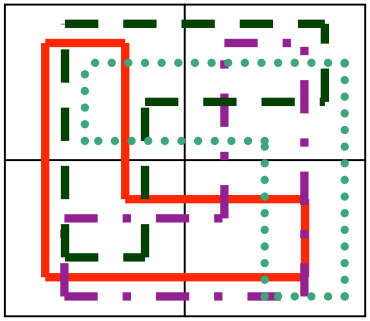
Backup Slides

- Fault Tolerance Mapping (continued)
  - Increases the dependability of the link layer operation within an FPGA
  - Overall architecture based on a priori knowledge of the failure within an FPGA.
  - General Failure Distribution model
    - Spatial Representation of FPGA to have Euclidean coordinates ***(x,y)***.
    - Let ***p(x,y)*** be the probability of a point in an FPGA failing (thermal effects, radiation effects, and manufacturing). The probability of corruption in a quadrant

$$P_i = \sum_{(x,y)\in r_i} p(x,y)$$

r is the set of possible available resources in FPGA

    - Redundant spatial variation of FPGA utilization (75% FPGA utilization). $P_1=P_2=P_3=P_4$



Link Layer Recognition and Processing Schemes – State Based Protocol Reconfiguration Algorithm (for HDLC & 802.3)

- **For sample case below with high Bit Error Rate (BER) - that the improvement is using a few samples for the single SNR case where there is extremely high bit error rate reduces the likelihood of making a reconfiguration error by a factor of ~533 times**

SNR	Majority Rule (Threshold Decision ONLY)	Weighted averaging using _T + 1 = 4	Weighted averaging using _T + 1 = 8
~0 dB	0.0016	6e-4	3e-4

For a BPSK waveform, we calculate the link layer detection of probability of mis-reconfiguration